

A TLA+ FORMAL SPECIFICATION AND VERIFICATION OF A NEW REAL-TIME COMMUNICATION PROTOCOL

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- 1 INTRODUCTION
- 2 DoRIS - A DOUBLE RING SERVICE FOR RTS
- 3 TLA+ FORMAL SPECIFICATIONS
- 4 CONCLUSION



1 INTRODUCTION

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DISTRIBUTED SYSTEM

- **System**: A set of station sharing a same communication bus (connected graph).
- **Capabilities**: messages, clocks and/or timers and processing capabilities

RESTRICTIONS

- No shared-memory
- No global clock



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DETERMINISTIC COMMUNICATION

- ▶ **Timeliness**: Temporal requirements of applications
- ▶ **Reliability**: Fault-tolerance

➡ **HARD MESSAGES**

HIGH THROUGHPUT

- ▶ Optimization and flexibility
- ▶ Diversity of the devices
- ▶ Reconfiguration of the system

➡ **SOFT MESSAGES**



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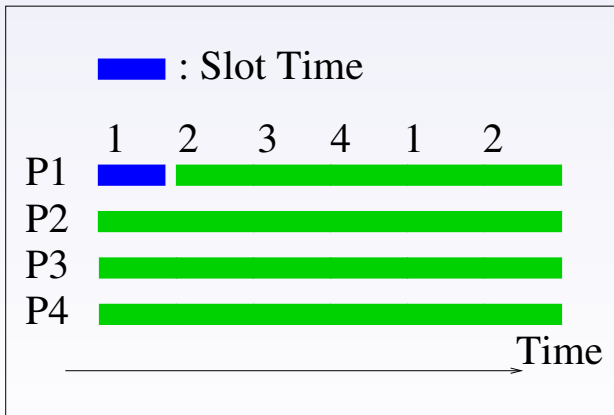
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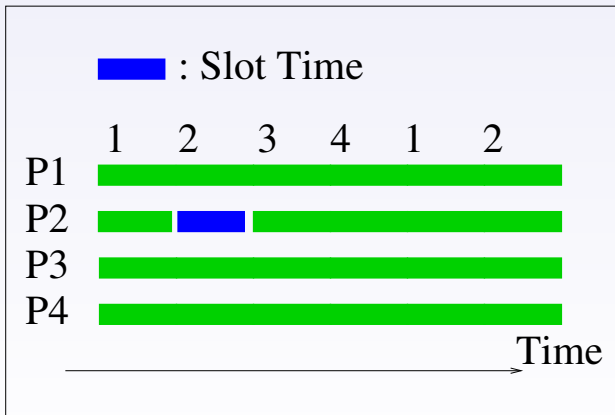
TDMA APPROACH - TIME DIVISION MULTIPLE ACCESS

- Periodic slots allocated to each process
- **Limitation**: Clocks synchronization, bandwidth waste



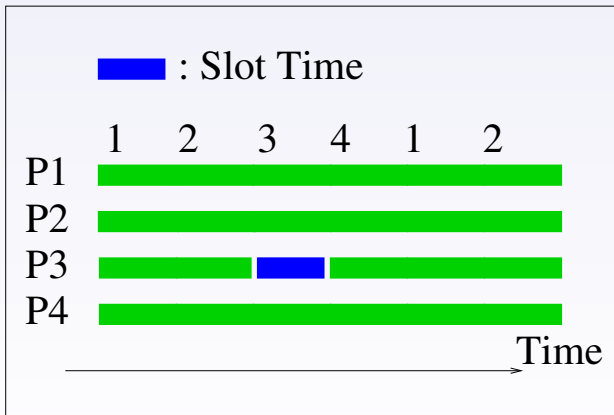
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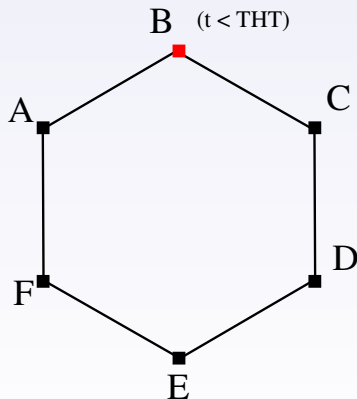
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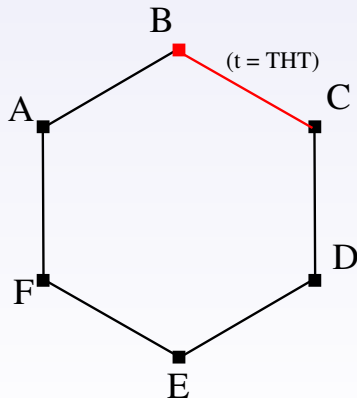
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- Token (explicit or not) \Rightarrow gives the right to transmit
- **Drawbacks:** Overload, token loss, variability



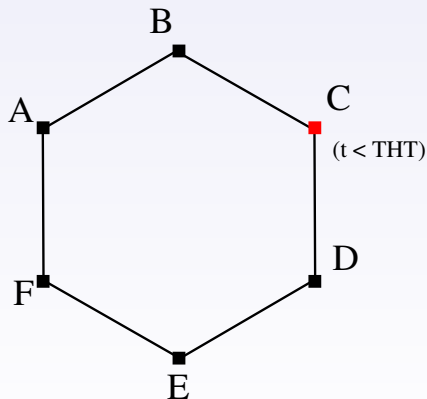
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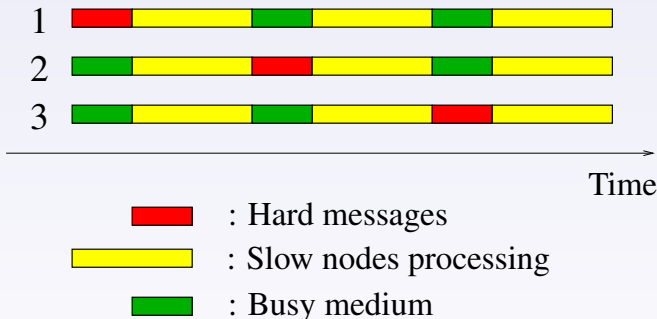


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PROCESSING DYNAMICS: SLOW VS FAST



FUNDAMENTAL PROPERTY

While **slow nodes** process hard messages
fast nodes use the available bandwidth for soft communication



SUMMARY

1 INTRODUCTION

2 DoRIS - A DOUBLE RING SERVICE FOR RTS

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DoRiS: COMPUTATIONAL MODEL - I

SERVERS

- *DoRiS* segment: $nServ$ nodes and **one** communication medium
- Each node hosts one *DoRiS* server, uniquely identified, responsible for hard and soft messages transmission
- *HardServ*[i] and *SoftServ*[i]: threads of server i dealing with the hard and soft queues, respectively

SYNCHRONOUS DISTRIBUTED SYSTEM

Regular and predictable points of synchronism

▮▮▮▮▶ Node clocks are synchronized

▮▮▮▮▶ **Global clock** emulation (despite our system model)

FAILURE

Crash failure and message omission failure

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- δ : hard message transmission time
(e.g. $64B \Rightarrow \approx 5\mu s$ over Fast-Ethernet)
- π : worst-case processing time of slow nodes

Assumption: $\delta \ll \pi$

COMMUNICATION MODEL

- Broadcast and publish-subscribe
- Soft messages of variable length
(e.g. $64B \leq L \leq 1500B$ over Ethernet).



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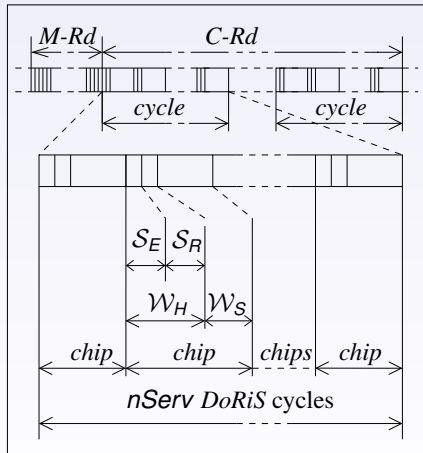
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DoRiS: TIME STRUCTURE



TIME

Membership Rounds (M-Rd) and Communication Rounds (C-Rd)

CYCLE

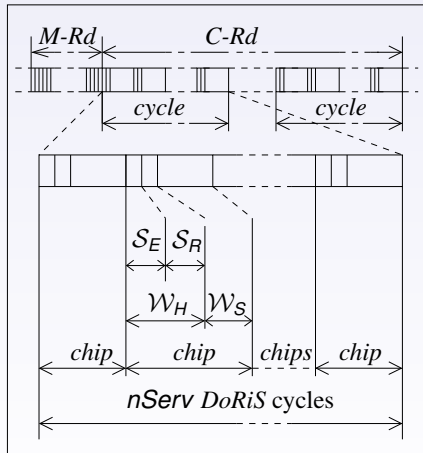
Sequence of $nServ$ chips (Δ_C)

CHIP

Hard (\mathcal{W}_H) and soft window (\mathcal{W}_S)

- \mathcal{W}_H ($2\Delta_E$): elementary (\mathcal{S}_E) and reservation slot (\mathcal{S}_R)
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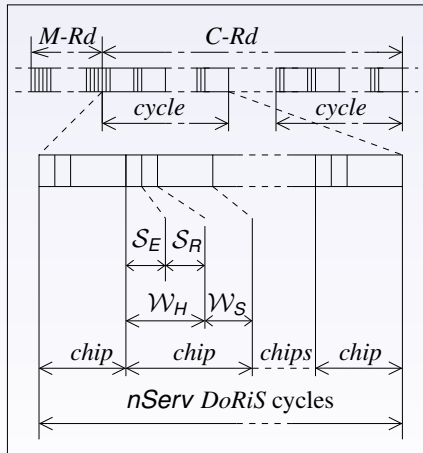
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ELEMENTARY MESSAGES

Mandatory 

Each server sends a **unique** elementary message per cycle

CONSEQUENCE

Periodicity 

Determinism, Synchrony (Global clock)
and **Fault Tolerance**

INFORMATIONS PIGGYBACKED ON ELEMENTARY MESSAGES

 Reservation mechanism gives hard ring **flexibility** ▸ Res. Mech.

 Dynamic management of process group membership ▸ Dyn. Group



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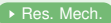
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FORMAL SPECIFICATION LANGUAGE

- Predicate logic, temporal Logic and Zermelo-Fraenkel set theory
- Allow for the specification of concurrent and distributed systems
- TLC: Temporal Logic Checker

CHARACTERISTICS

- Modular structure: allows for an incremental process of specification, according to the abstraction level required
- Concrete specification, close to the code level



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TIME MODEL

- Time: one more variable \Rightarrow State number increase
- Representation by naturals \Leftrightarrow Discrete increments
- Synchronous system (timers without jitter nor drift) \Leftrightarrow global clock

MAIN FORMULA

$$Spec \triangleq Init \wedge \Box[Next \vee Tick]_{vars} \wedge Liveness$$

- *Init*: the initial protocol states
- $\Box[Next \vee Tick]_{vars}$: the next-state relation
- *Liveness* $\triangleq \Box\Diamond Tick$: condition that ensures the progress of the behavior



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MAIN ACTIONS

$$\begin{aligned} \text{Next} \triangleq & \quad \vee \exists s \in \text{HardRing} : \text{ElemSend}(s) \vee \text{ReseSend}(s) \\ & \quad \vee \exists t \in \text{SoftRing}(\text{Shared.soft}) : \text{SoftSend}(t) \\ & \quad \vee \exists \text{msg} \in \text{Shared.medium} : \text{Receive}(\text{msg}) \end{aligned}$$
$$\text{Tick} \triangleq \text{NextTick} \vee \text{NextChip}$$

ElemSend, *ReseSend*
and *SoftSend*



Message emission actions

Receive (*HardRecv*
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Message reception action

NextTick and *NextChip*



Time passing actions

The complete specification is [Here](#)

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DoRiS: TLC VERIFICATION PERFORMANCE - I

SET-UP

2 Ghz Intel Core Duo processor, JVM with a 512M heap size

- 3 Metrics:
- CPU user time (U)
 - Total number of generated distinct states (N)
 - Diameter (D) of the reachability graph

RESULTS

	# Servers						
	2	4	6	8	10	12	14
U (seconds)	3	21	59	153	329	833	4,117
N (#states)	853	2,529	3,565	5,032	6,430	8,148	9,540
D (#states)	850	2,516	3,486	5,003	6,392	8,099	9,482



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REDUCED STATE NUMBER


- Temporal guards of actions
- Communication and fault scenarios fixed
- Time increment strategy (*NextTick* )

COMPARISON WITH NAIVE STRATEGY: UNIT TIME INCREMENTS

- 6 servers: $U = 453s(59s)$, $N = 21,604(3,565)$ and $D = 11,261(3,486)$
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ESSENTIAL *DoRiS* TEMPORAL PROPERTIES

► Temp. Prop.

- Correctness of the Hard Ring
- Correctness of the Reservation Mechanism
- Fairness of the Soft Ring

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- Specification and conception: interactive process
- Protocol drawbacks detected by model-checking the specification

FAULT TOLERANCE

- Fault occurrences were specified in incremental steps
- Straightforward process in TLA+

IMPLEMENTATION

- Specification: gives insights to carry out the implementation
- But, complexity of the Linux-based real-time operating system



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SPECIFICATION OF A NEW REAL-TIME COMMUNICATION PROTOCOL

- TLA+ specification of the *DoRiS* protocol
- Verification of *DoRiS* and its temporal properties by TLC

SOFTWARE ENGINEERING PERSPECTIVE

- Interactive design methodology: specification vs conception
- Implementation has been greatly improved

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7 DoRIS: CONSTANTS AND VARIABLES

8 DoRIS: ACTIONS





L. Lamport

Specifying Systems: The TLA+ language and tools for hardware and software engineers

Addison Wesley, 2002



F. B. Carreiro, J. A. Fonseca and P. Pedreiras

Virtual Token-Passing Ethernet - VTPE

Proc. FeT2003 5th IFAC Int. Conf. on Fieldbus Systems and their Applications, 2003



- Each server holds a reservation vector
- Elementary messages piggyback a reservation list
- Each server can reserve all free slots of the next cycle (its horizon)
- There always is a reservation slot available in a server horizon

FAULT TOLERANCE MECHANISM

- A server is consistent if it has received the previous $nServ$ elementary messages
- A server can reserve more than one reservation slot of its horizon
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DoRiS: DYNAMIC MANAGEMENT OF PROCESS GROUP MEMBERSHIP

◀ Back

- Elementary messages piggyback a flag bit
- Each server holds a list with its view of the process group membership
- Upon receiving an elementary message, each server updates the process group membership

FAULT TOLERANCE MECHANISM

- Elementary message omission failure \Rightarrow The server loose its right to send soft messages
- After an empty window \mathcal{W}_S , all servers update the process group membership to the empty set



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A computation of a system is represented by a sequence of states.

DEFINITIONS

State	\triangleq	Assignment of constant values to variables
Behavior	\triangleq	Sequence of states
Predicate	\triangleq	Formula which contains variables of only one state
Step $S : i \rightarrow f$	\triangleq	pair of consecutive states i and f
Transition function	\triangleq	Formula which contains variables of both state i e f
Action	\triangleq	Boolean-valued transition function on steps



The prime ($'$) operator is used to distinguish the values of variables on steps. Let $S : i \rightarrow f$ be a step:

- v : value of v in state i
- v' : value of v in state f

EXAMPLE

- $v = 0$ in i and $v = 1$ in f ($v' = 1$)
- $[v' - v]$ is a transition function
- $[v' - v]$ equals 1 on S
- $[v' = v + 1]$ is an action true on S



NEXT-STATE RELATION

The next-state relation associated to step $S : i \rightarrow f$ is the set of actions defined on S .

THE \square OPERATOR

In a behavior Σ , an action A is true, denoted $\square[A]_{vars}$ $\Leftrightarrow \forall S : i \rightarrow f$ of Σ that alters the set $vars$ of all variables, A is true on S



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Constants	Description
$nServ$	Number of <i>DoRiS</i> servers of a <i>DoRiS</i> segment
δ_{chip}	Duration (Δ_C) of a chip
δ	Transmission time (δ) of a hard message
π	Processing time (π) of a hard message by the slowest device
$maxTxTime$	Transmission time of the largest message
$horiz$	Number of total cycles used to check a <i>DoRiS</i> model



SHARED

Field	Description
<i>soft</i>	set of servers participating of the soft communication.
<i>chipTimer</i>	increasing timer, ranging from 0 to Δ_C , that represents the flow of time during a chip.
<i>chipCount</i>	counter that identifies each chip, modulo $nTask$.
<i>cycleCount</i>	counter that identifies each cycle, modulo $nCycle$.
<i>medium</i>	if no message is being transmitted, <i>medium</i> equals $\{\}$. Else, <i>medium</i> stores the message being transmitted.
<i>macTimer</i>	decreasing timer that specifies the time remaining in order to complete an on-going message transmission. As a special case, $macTimer = 0 \Rightarrow medium = \{\}$.



HARDSTATE

Field	Description
<i>msg</i>	list of hard messages stored in local buffers after their reception by the network device.
<i>execTimer</i>	decreasing timer that specifies the time remaining in order to complete the processing of a hard message.
<i>res</i>	reservation list for the <i>nServ</i> next chips.
<i>cons</i>	counter that represents the number of elementary messages received in a complete <i>DoRiS</i> cycle.



SOFTSTATE

Field	Description
<i>token</i>	counter used to rule the token circulation during \mathcal{W}_S .
<i>list</i>	list of soft messages waiting to be transmitted.
<i>count</i>	the number of soft messages received during a \mathcal{W}_S window.

HISTORY

Field	Description
<i>elem</i>	the number of elementary messages sent in a cycle.
<i>rese</i>	the number of reservation messages sent in a cycle.



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$$\begin{aligned}
 ElemSend(s) &\triangleq \quad \wedge Shared.medium = \{\} \wedge Shared.chipTimer = 0 \\
 &\wedge LET \quad i \quad \triangleq \quad hardID(s) \\
 &\quad flag \triangleq \quad IF SoftState[i].list \neq \langle \rangle \text{ THEN } 1 \text{ ELSE } 0 \\
 IN \quad &\wedge Shared.chipCount = i \\
 &\wedge LET \quad resSet \triangleq \quad reservation(i) \\
 IN \quad &\wedge Shared' = [Shared \text{ EXCEPT} \\
 &\quad \quad !.macTimer = delta, \\
 &\quad \quad !.medium = \{[id \mapsto i, type \mapsto \text{"hard"}, \\
 &\quad \quad \quad \quad res \mapsto resSet, softFlag \mapsto flag]\}] \\
 &\wedge HardState' = [HardState \text{ EXCEPT} \\
 &\quad \quad ![i].cons[i] = 1, \\
 &\quad \quad ![i].res = [j \in ServID \mapsto IF j \in resSet \text{ THEN } i \text{ ELSE } @[j]]] \\
 &\wedge SoftState' = [SoftState \text{ EXCEPT} \\
 &\quad \quad ![i].token = IF flag = 0 \text{ THEN } -1 \text{ ELSE } @] \\
 &\wedge History' = [History \text{ EXCEPT } !.elem = @ + 1]
 \end{aligned}$$


$$\begin{aligned}
\text{ReseSend}(s) \triangleq & \\
& \wedge \text{Shared.medium} = \{\} \\
& \wedge \text{Shared.chipTimer} = \text{delta} \\
& \wedge \text{LET } i \triangleq \text{hardID}(s) \\
& \text{IN } \wedge \text{HardState}[i].\text{res}[\text{Shared.chipCount}] = i \\
& \wedge \text{Shared}' = [\text{Shared} \text{ EXCEPT} \\
& \quad !.\text{macTimer} = \text{delta}, \\
& \quad !.\text{medium} = \{[id \mapsto i, \text{type} \mapsto \text{"hard"}, \text{res} \mapsto \{-1\}]\}] \\
& \wedge \text{HardState}' = [j \in \text{ServID} \mapsto [\text{HardState}[j] \text{ EXCEPT} \\
& \quad !.\text{res}[\text{Shared.chipCount}] = -1]] \\
& \wedge \text{History}' = [\text{History} \text{ EXCEPT } !.\text{rese} = @ + 1] \\
& \wedge \text{UNCHANGED } \text{SoftState}
\end{aligned}$$


$$\begin{aligned}
 \text{SoftSend}(s) &\triangleq \quad \wedge \text{Shared.medium} = \{\} \\
 &\quad \wedge 2 * \text{delta} \leq \text{Shared.chipTimer} \wedge \text{Shared.chipTimer} \leq \text{deltaChip} \\
 &\quad \wedge \text{LET } i \quad \triangleq \quad \text{softID}(s, \text{Shared.soft}) \\
 &\quad \quad \text{lenTX} \triangleq \text{lenMsg}(i) \\
 &\quad \quad d \triangleq \text{Shared.chipTimer} + \text{lenTX} \\
 &\quad \quad \text{consis} \triangleq \forall j \in \text{ServID} : \text{HardState}[i].\text{cons}[j] = 1 \\
 &\quad \quad \text{wait} \triangleq (d > \text{deltaChip}) \vee (\neg \text{consis}) \\
 &\quad \quad \text{noMsg} \triangleq (i \in \text{Failed}) \vee \text{wait} \\
 \text{IN} \quad &\quad \wedge i = \text{SoftState}[i].\text{token} \wedge \text{Shared}' = [\text{Shared} \text{ EXCEPT} \\
 &\quad \quad ! .\text{macTimer} = \text{IF noMsg THEN Infinity ELSE lenTX}, \\
 &\quad \quad ! .\text{medium} = \text{IF noMsg THEN @ ELSE } \{[id \mapsto i, \text{type} \mapsto \text{"soft"}]\} \\
 &\quad \wedge \text{SoftState}' = [\text{SoftState} \text{ EXCEPT} \\
 &\quad \quad ![i].\text{list} = \text{IF wait THEN @ ELSE tailList}(@), \\
 &\quad \quad ![i].\text{token} = \text{CASE wait} \rightarrow @ \square \neg \text{consis} \rightarrow -1 \\
 &\quad \quad \quad \square \text{OTHER} \rightarrow \text{next}(i, \text{Shared.soft}), \\
 &\quad \quad ![i].\text{count} = \text{IF noMsg THEN @ ELSE @ + 1}] \\
 &\quad \wedge \text{UNCHANGED } \langle \text{HardState}, \text{History} \rangle
 \end{aligned}$$


$HardRecv(m) \triangleq$

$\wedge \text{CASE } m.res \neq \{-1\} \wedge m.softFlag = 1$

$\rightarrow \wedge Shared' = [Shared \text{ EXCEPT } !.medium = \{\}, !.soft = @ \cup \{m.id\}]$
 $\wedge \text{UNCHANGED } SoftState$

$\square m.res \neq \{-1\} \wedge m.softFlag = 0$

$\rightarrow \wedge Shared' = [Shared \text{ EXCEPT } !.medium = \{\}, !.soft = @ \setminus \{m.id\}]$
 $\wedge tokenUpdate(m)$

$\square m.res = \{-1\}$

$\rightarrow \wedge Shared' = [Shared \text{ EXCEPT } !.medium = \{\}]$
 $\wedge \text{UNCHANGED } SoftState$



Continue

$$\begin{aligned}
 \wedge \text{HardState}' = & \\
 & [i \in \text{NoRecvSet}(m) \mapsto \text{HardState}[i]] @@ \\
 & [i \in \text{ServID} \setminus \text{NoRecvSet}(m) \mapsto [\text{HardState}[i] \text{ EXCEPT} \\
 & \quad \text{!.execTimer} = \text{IF } \text{Len}(\text{HardState}[i].\text{msg}) = 0 \text{ THEN } pi \text{ ELSE } @, \\
 & \quad \text{!.cons}[m.\text{id}] = \text{IF } m.\text{res} \neq \{-1\} \text{ THEN } 1 \text{ ELSE } @, \\
 & \quad \text{!.msg} = \text{Append}(@, m), \text{!.res} = \\
 & \quad \quad \text{IF } m.\text{res} = \{-1\} \\
 & \quad \quad \text{THEN } [j \in \text{ServID} \mapsto \text{IF } j = m.\text{id} \text{ THEN } -1 \text{ ELSE } @[j]] \\
 & \quad \quad \text{ELSE } [j \in \text{ServID} \mapsto \text{IF } j \in m.\text{res} \text{ THEN } m.\text{id} \text{ ELSE } @[j]]]] \\
 \wedge \text{UNCHANGED } \text{History}
 \end{aligned}$$


$$\text{SoftRecv}(m) \triangleq$$

$$\wedge \text{LET } \text{lastSoft} \triangleq \wedge 2 * \text{delta} \leq \text{Shared.chipTimer}$$

$$\wedge \text{Shared.chipTimer} \leq \text{deltaChip}$$

$$\wedge \forall j \in \text{ServID} : \text{SoftState}[j].\text{token} = -1$$

$$\text{IN } \text{Shared}' = [\text{Shared} \text{ EXCEPT}$$

$$\quad \text{!.medium} = \{\},$$

$$\quad \text{!.macTimer} = \text{IF } \text{lastSoft} \text{ THEN } \text{Infinity} \text{ ELSE } @,$$

$$\quad \text{!.soft} = \text{IF } \text{lastSoft} \text{ THEN } \{\} \text{ ELSE } @@]$$

$$\wedge \text{SoftState}' = [j \in (\text{ServID} \setminus \text{Shared.soft}) \cup \{m.\text{id}\} \mapsto \text{SoftState}[j]] @@$$

$$[j \in \text{Shared.soft} \setminus \{m.\text{id}\} \mapsto [\text{SoftState}[j] \text{ EXCEPT}$$

$$\quad \text{!.token} = \text{next}(@, \text{Shared.soft}),$$

$$\quad \text{!.count} = @ + 1]]$$

$$\wedge \text{UNCHANGED } \langle \text{HardState}, \text{History} \rangle$$


$Receive(m) \triangleq$

$\wedge \text{Shared.macTimer} = 0$

$\wedge \text{CASE } m.type = \text{"hard"} \rightarrow \text{HardRecv}(m)$

$\square m.type = \text{"soft"} \rightarrow \text{SoftRecv}(m)$



$$NextTick \triangleq$$

$$LET \ noRese \triangleq \wedge Shared.medium = \{\}$$

$$\wedge Shared.chipTimer = delta$$

$$\wedge \forall i \in ServID : HardState[i].res[Shared.chipCount] \neq i$$

$$noSoft \triangleq \wedge 2 * delta \leq Shared.chipTimer$$

$$\wedge Shared.chipTimer \leq deltaChip$$

$$\wedge Shared.medium = \{\}$$

$$\wedge \forall j \in Shared.soft : SoftState[j].token \neq j$$

$$tmp \triangleq \{HardState[i].execTimer : i \in ServID\} \cup$$

$$\{deltaChip - Shared.chipTimer\}$$

$$d \triangleq minIncVal(tmp, noRese, noSoft)$$

$$IN \quad \wedge d > 0$$

$$\wedge timerUpdate(d, noRese, noSoft)$$

$$\wedge UNCHANGED \langle SoftState, History \rangle$$




CORRECTNESS OF THE HARD RING

$$\text{HardRingCorrectness} \triangleq$$

$$\begin{aligned} & \wedge \forall s \in \text{HardRing} : \Box(\text{Len}(\text{HardState}[\text{hardID}(s)].\text{msg}) \leq 3) \\ & \wedge \Box(\text{ENABLED NextChip} \Rightarrow \text{History.elem} = \text{Shared.chipCount}) \end{aligned}$$

CORRECTNESS OF THE RESERVATION MECHANISM

$$\text{ReservationSafety} \triangleq$$

$$\begin{aligned} & \Box \forall \text{chip}, j \in \text{ServID} : \wedge \text{ENABLED ReseSend}(\text{HardServ}[j]) \\ & \quad \wedge \text{Shared.chipCount} = \text{chip} \\ \Rightarrow & \quad \wedge \text{HardState}[j].\text{res}[\text{chip}] = j \\ & \quad \wedge \forall i \in \text{ServID} \setminus \{j\} : \text{HardState}[i].\text{res}[\text{chip}] \in \{j, -1\} \end{aligned}$$



FAIRNESS OF THE SOFT RING

$$\text{SoftRingFairness} \triangleq$$

$$\begin{aligned} & \wedge \forall i \in \text{ServID} : \square(i \in \text{Shared.soft} \\ & \quad \Rightarrow (\text{SoftState}[i].\text{list} \neq \langle \rangle \Rightarrow \diamond(i = \text{SoftState}[i].\text{token}))) \\ & \wedge \square \diamond (\forall i \in \text{ServID} \setminus \text{Failed} : i \in \text{Shared.soft} \\ & \quad \Rightarrow \text{Len}(\text{SoftState}[i].\text{list}) = 0) \end{aligned}$$

